L–C-Band Low-Voltage BiCMOS MMIC's for Dual-Mode Cellular–LAN Applications

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***Abstract*— This paper is concerned with the design considerations and performance results for low-voltage Si monolithic microwave/millimeter-wave integrated circuits (MMIC's) developed for mobile and personal communications applications. A 0.4 μm ECL–BiCMOS process technology was employed to develop bipolar-based RF amplifiers, MOS-based IF amplifiers, BiCMOS-based simplified Gilbert mixers, and monolithic downconverter as well as upconverter IC's incorporating these elements. These converters are designed to operate at a bias voltage of 2 V over 1.8–6.2 GHz exhibiting a conversion gain of 35–15 dB with a variable IF frequency of up to several 100 MHz. Chip size for both the downconverter and upconverter IC's is 1.0 mm × 0.7 mm.**

I. Introduction

RECENT advances in cellular phone and wireless network technologies, including 1.9 GHz PCS and DECT, 2.4 GHz ISM band WAN, and 5.2 GHz Hiperlan [1] have urged development of low-cost, small-size, low-power fully monolithic RF/IF modules covering the above frequency bands. Presently available modules operate with 3–6 V dc voltage and can offer a maximum bit rate of 2 Mbps [2]–[4]. There are also some attempts recently reported to achieve RF modules operating with 1.9–2.7 V dc voltage [5]–[7]. However, all these modules can operate over a frequency range of 1.5–2.5 GHz with an IF frequency of up to 100 MHz. To facilitate high-speed transmission of voice, data, and video in such a personal wireless system, and to enable development of a dual-mode PCMCIA card for cellular—LAN system application, achievement of low-power 2 V-class downconverter/upconverter modules covering the full frequency range of 1.9–5.2 GHz with IF frequencies in the several MHz to several 100 MHz range is indispensable.

The present paper combines high frequency potential features of bipolar transistors with low power characteristics of MOS devices in an optimized circuit design, to realize downconverter and upconverter chips operating at 2 V and covering the 1.8–6.2 GHz frequency range with a variable IF frequency of up to several 100 MHz.

Manuscript received July 26, 1995; revised July 22, 1996.

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Publisher Item Identifier S 0018-9480(96)07917-3.

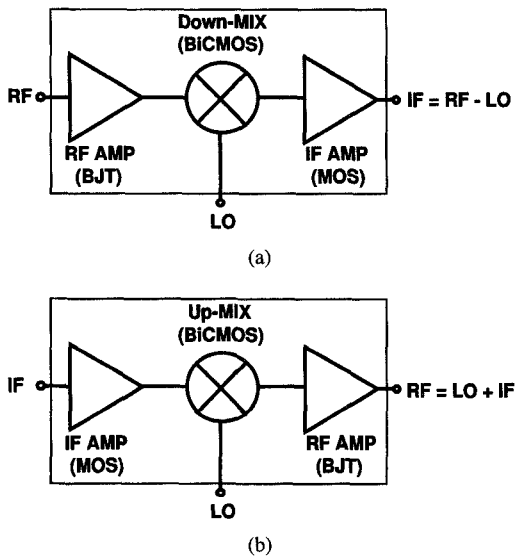


Fig. 1. Block diagrams of (a) downconverter and (b) upconverter.

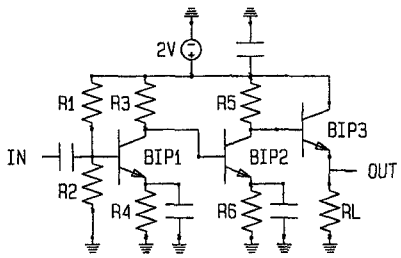


Fig. 2. Equivalent circuit for RF amplifier.

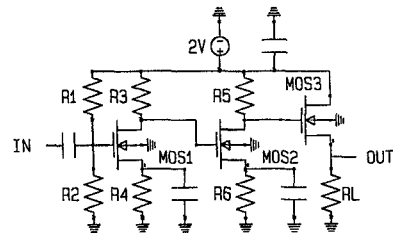
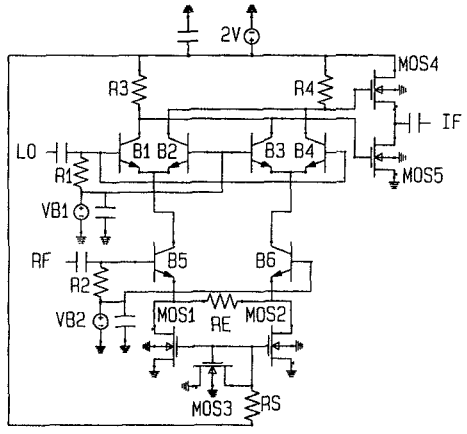


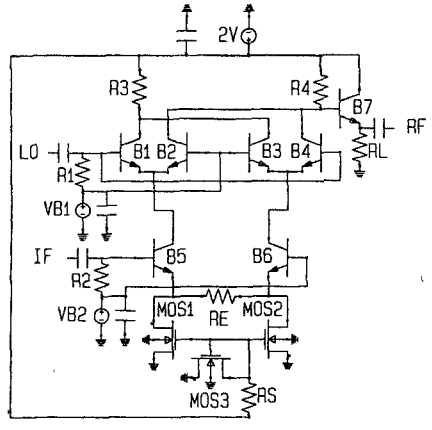
Fig. 3. Equivalent circuit for IF amplifier.

II. Circuit Design

Block diagrams for the downconverter and upconverter modules are shown in Fig. 1. Each module consists of an RF amplifier, an IF amplifier, and a mixer. Applying several SPICE simulations, we adopted an optimum selection of



(a)



(b)

Fig. 4. Equivalent circuits for (a) downconverter's mixer and (b) upconverter's mixer.

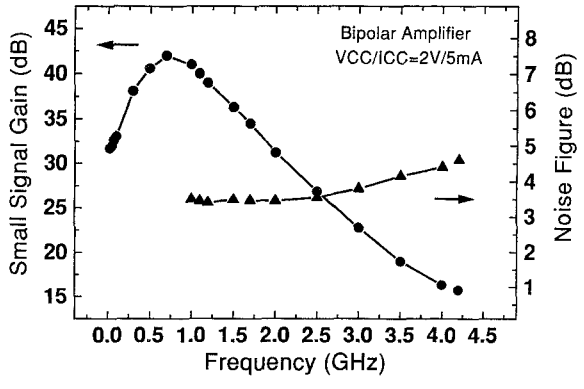


Fig. 5. Small signal gain and noise figure for RF amplifier.

bipolar and MOS technologies for different stages in the RF and IF amplifiers, as well as the mixer, for:

1) achieving the highest conversion gain at a nominal supply voltage of 2 V;
2) obtaining a wide RF bandwidth covering 1.8–6.2 GHz, and a wide IF bandwidth covering up to 1000 MHz; and
3) suppressing the local oscillator (LO) and other unnecessary signals, without employing a particular filtering circuit which otherwise increases the chip size. Moreover, a high impedance interstage matching design approach

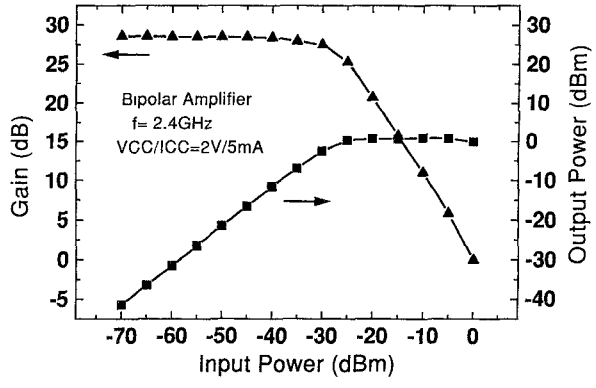


Fig. 6. Input-output power characteristics for RF amplifier.

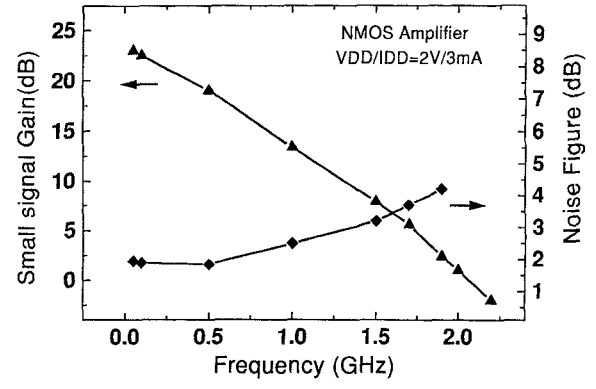


Fig. 7. Small signal gain and noise figure for IF amplifier.

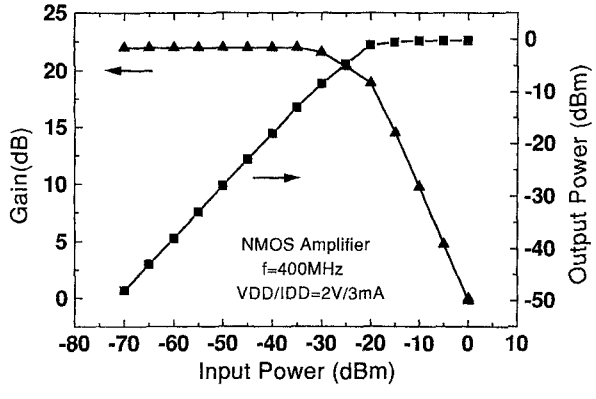


Fig. 8. Input-output power characteristics for IF amplifier.

was applied for keeping the power consumption low, and avoiding conversion gain degradation.

A. RF Amplifier

An equivalent circuit for the RF amplifier is shown in Fig. 2. To enhance a high frequency operation for the downconverter and the upconverter, a bipolar-based circuit topology was adopted for the RF amplifier. The amplifier has a simple 2-stage common emitter configuration followed by an emitter follower buffer stage. The emitter area for bipolar transistors BIP1 and BIP2 in the common emitter stages is $0.8\,\mu\text{m} \times 6.4\,\mu\text{m}$, while the emitter size for transistor BIP3 in the buffer stage is twice that for the common emitter stage to increase the amplifier output level.

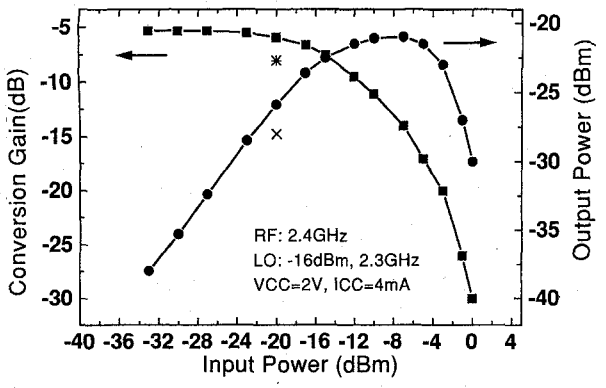
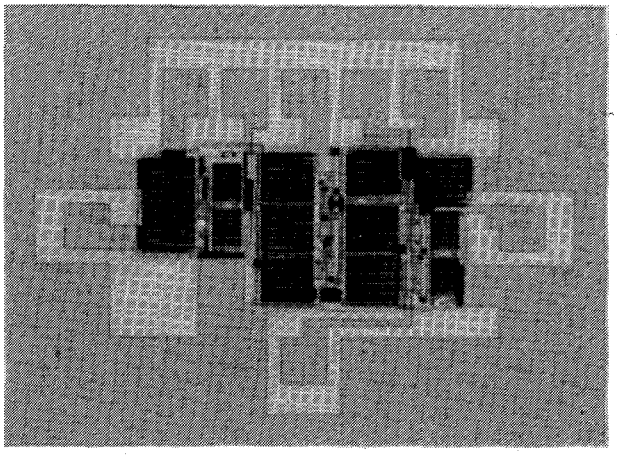
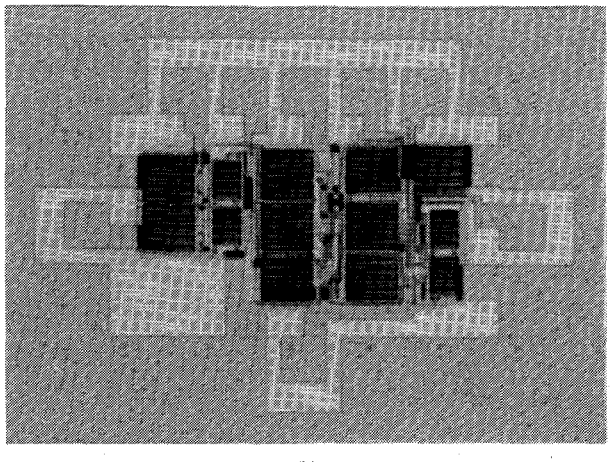


Fig. 9. Mixers' performance versus input power level.

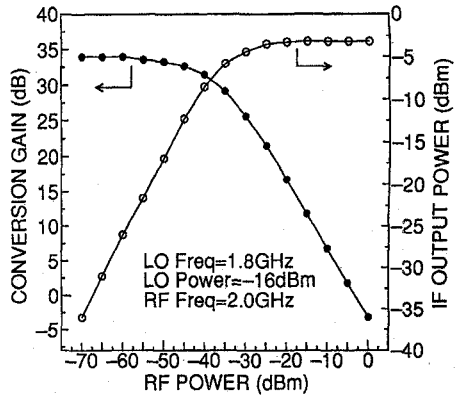


(a)

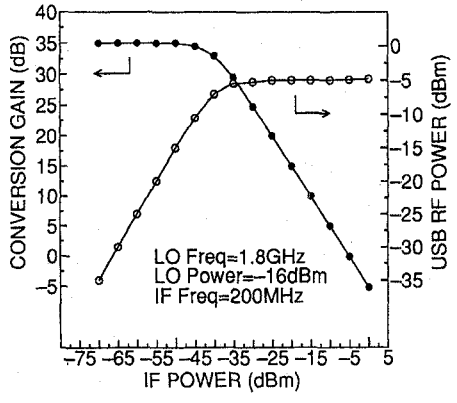


(b)

Fig. 10. Chip photographs for (a) downconverter and (b) upconverter.



(a)



(b)

Fig. 11. (a) Downconverter and (b) upconverter performance versus input power.

B. IF Amplifier

An equivalent circuit for the IF amplifier is shown in Fig. 3. The IF amplifier resembles the RF amplifier but utilizes NMOS transistors which require less dc power and can provide sufficient gain for the IF signal frequency range. The IF amplifier is also responsible for attenuating high frequency components at the amplifier's output port, through optimization of an RC-filter realized by parallel combination of bias resistors R1 and R2, and the gate-source capacitance of the first common source transistor MOS1. Gate length and width for transistors MOS1 and MOS2 in the common source stages are, respectively, 0.4 μm and 50 μm. Gate width for transistor MOS3 in the buffer stage is twice that for the common source to enhance output power.

C. Mixers

Equivalent circuits for the mixers used in each frequency converter are presented in Fig. 4. To assure a 2 V dc power operation and low LO power requirement, a simplified Gilbert cell was adopted, and voltage drop distribution for load resistors R3, R4, series-gated transistors B1 to B6, and current source transistors MOS1, MOS2 in the cell was optimized based on a SPICE simulation. Use is made of bipolar transistors in the cell which is responsible for a high frequency mixing of the LO and RF signals. A current source circuit for each mixer employs NMOS transistors for their low power requirement and applicability as a power control device. To realize a 2 V operation, voltage drops for the NMOS, each bipolar transistor in the series-gated cell, and the load resistor are 0.7, 0.5, and 0.3 V, respectively, under a condition that reference voltages VB1 and VB2 are adjusted to provide a collector current equal to 4 mA. The mixer in the downconverter module utilizes an NMOS push-pull buffer stage, while the mixer in the upconverter module uses a bipolar emitter

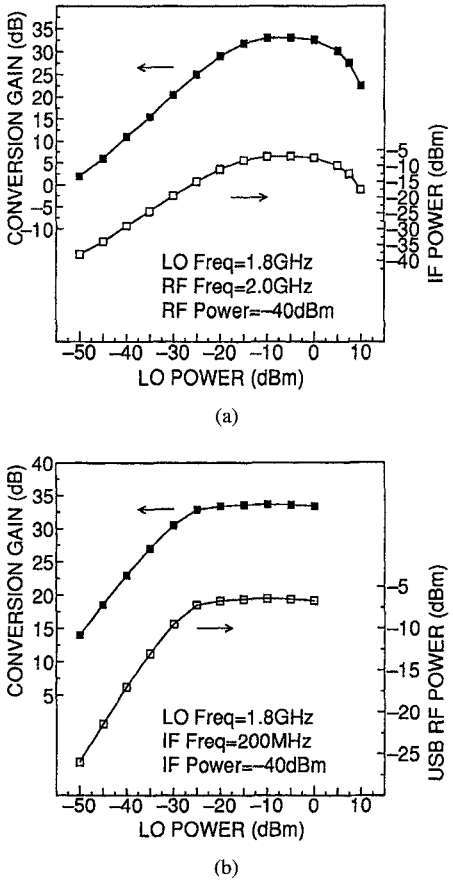


Fig. 12. (a) Downconverter and (b) upconverter performance versus LO power.

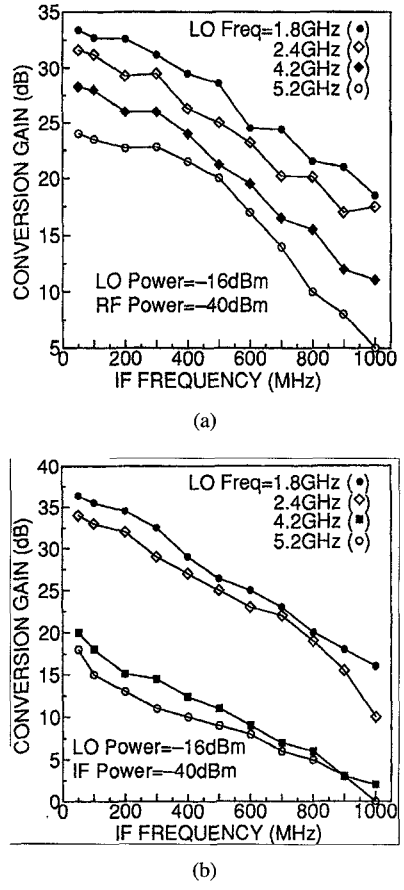


Fig. 13. (a) Downconverter and (b) upconverter performance versus IF frequency with LO frequency as a parameter.

follower buffer stage. Emitter area for a bipolar transistor in the mixers is $0.8\,\mu\text{m} \times 6.4\,\mu\text{m}$, and gate area for an NMOS is $0.4\,\mu\text{m} \times 50\,\mu\text{m}$.

D. Filtering

The present downconverter and upconverter modules make use of no particular on-chip or off-chip filter for suppressing unnecessary signals at the output port. As it was stated earlier, high frequency filtering characteristics of NMOS push-pull buffer stage in the downconverter module's mixer and an optimized RC-filtering feature of the NMOS IF amplifier are utilized to realize excellent isolation characteristics for each module.

III. Fabrication Process and Device Characteristics

The chips were fabricated employing a $0.4\,\mu\text{m}$ ECL–BiCMOS process technology which has been developed for high speed digital circuit applications [8]. The bipolar transistor has a double polysilicon self-aligned emitter-base structure, and an NMOS transistor has a WSi/polysilicon gate LDD structure. To fabricate the load and bias resistors, polysilicon layers with different sheet resistances were used, and to fabricate bypass and dc blocking capacitances, a poly-to-poly structure was employed. A $0.8\,\mu\text{m} \times 6.4\,\mu\text{m}$ bipolar transistor has a typical β and f_T of, respectively, 40 and 20 GHz at a collector voltage of 1 V. A $0.4\,\mu\text{m} \times 50\,\mu\text{m}$ NMOS transistor, on the other hand, has a typical V_T and I_{ON} of, respectively, 0.5 V and 21 mA at a drain voltage of 3.3 V. Measured f_T for the NMOS is 15 GHz which has been obtained for a drain voltage and current of 3.3 V and 5 mA.

IV. Microwave Performance

On-wafer Cascade Microtech probes were utilized to evaluate microwave performance for developed bipolar and MOS amplifiers, mixers, and converter chips.

A. RF Amplifier

Measured small signal gain and noise figure characteristics, as well as input power dependence at a frequency of 2.4 GHz for the RF amplifier are, respectively shown in Figs. 5 and 6. The amplifier draws 5 mA from a 2 V bias supply to exhibit a small signal power gain higher than 15 dB, and a noise figure lower than 4 dB for a frequency of up to 4 GHz. The output power at 1-dB gain compression point is about 0 dBm for an input signal frequency of 2.4 GHz.

B. IF Amplifier

Measured small signal gain and noise figure characteristics, as well as input power dependence at a frequency of 400 MHz for the IF amplifier are, respectively shown in Figs. 7 and 8. The amplifier draws 3 mA from a 2 V bias supply to exhibit a

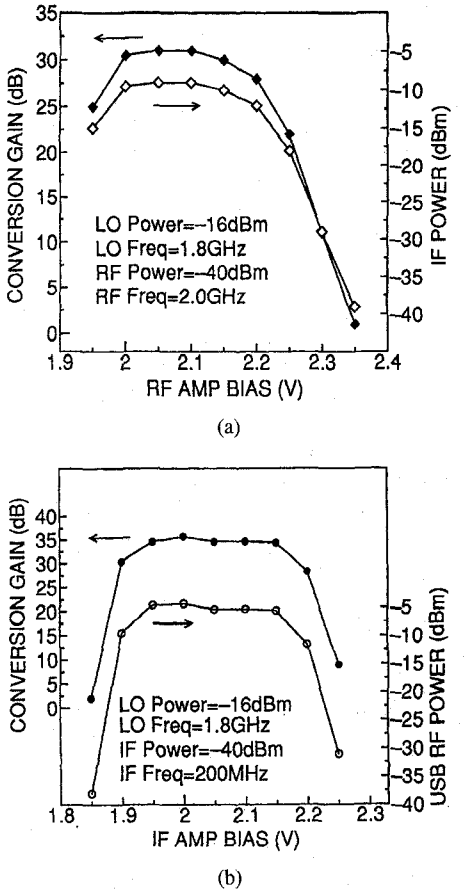


Fig. 14. (a) Downconverter and (b) upconverter performance versus dc bias change.

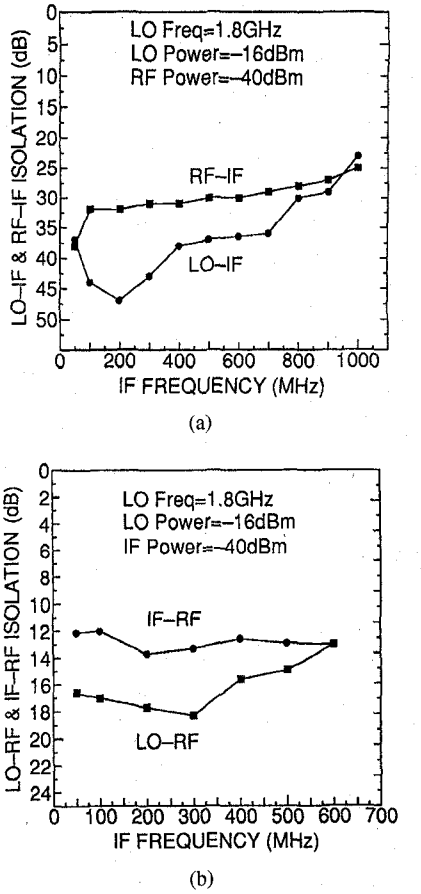


Fig. 15. (a) Downconverter and (b) upconverter port-to-port isolation characteristics.

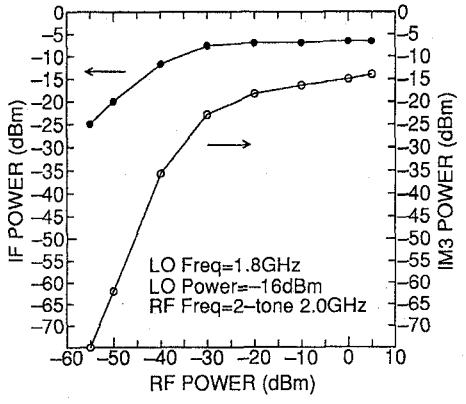
small signal power gain higher than 13 dB, and a noise figure lower than 2.5 dB for a frequency of up to 1 GHz. The output power at 1-dB gain compression point is about −5 dBm for an input signal frequency of 400 MHz.

C. Mixers

For an LO frequency and power level of 2.3 GHz and −16 dBm and an RF frequency of 2.4 GHz, input power dependence of the conversion gain and output power for the mixers used in the downconverter and upconverter chips were investigated. Results are shown in Fig. 9. Block circles and squares, respectively, represent the conversion gain and output power for the downconverter mixer, while the asterisk and plus signs represent, respectively those for the upconverter mixer. Both mixers exhibit a small signal conversion gain of higher than −8 dB for an input power lower than −20 dBm, under a 2 V bias condition.

D. Downconverter and Upconverter

Chip microphotograph for each frequency converter module is shown in Fig. 10. Chip size for both the downconverter and upconverter modules is 1.0 mm × 0.7 mm. Fig. 11 depicts conversion gain as well as output power variation versus input power for an LO frequency of 1.8 GHz and an LO power of −16 dBm. The developed modules exhibit an input dynamic range of 40 dB. Maximum conversion gain for the downconverter and the upconverter modules is, respectively, 34 and 35 dB. Fig. 12 represents conversion gain and output power against LO power for an LO frequency of 1.8 GHz and an input power level of −40 dBm. The converters operate with an LO power level as low as −40 dBm, and maximum conversion gain is obtained at an LO power of −16 and −10 dBm, respectively, for the downconverter and upconverter. Performance of the downconverter and upconverter chips versus the IF frequency, for an input power of −40 dBm, an LO power of −16 dBm, and the LO frequency as a parameter, is shown in Fig. 13. Noting that RF = LO + IF, both chips can cover the 1.8–6.2 GHz band with an IF frequency up to 1000 MHz and sufficient conversion gain. Fig. 14 shows conversion gain and output power versus RF amplifier bias voltage for the downconverter, and IF amplifier bias voltage for the upconverter. While the maximum conversion gain is achieved for a dc voltage of 2.05–2.10 V, both chips exhibit a graceful degradation for a ±0.15 V voltage deviation. As shown in Fig. 15, measured LO–IF and RF–IF isolation for the downconverter is better than 30 dB for an IF frequency of up to 500 MHz, and better than 23 dB for an IF frequency of up to 1000 MHz. On the other hand, maximum LO–RF and IF–RF isolation for the upconverter is, respectively, 18 and 14 dB. Third order intermodulation product power levels for the downconverter and upconverter were measured to be 5 dBm, as indicated in Fig. 16. Power dissipation for each frequency converter module is 24 mW.



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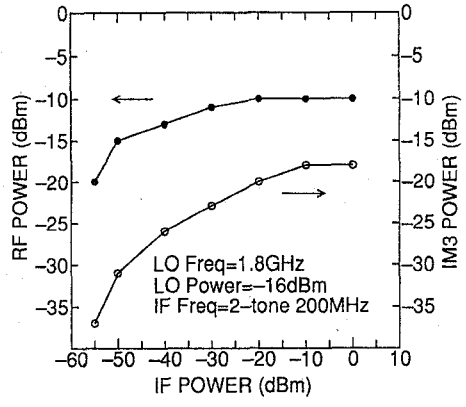

(b)

Fig. 16. (a) Downconverter and (b) upconverter 3rd order intermodulation characteristics.

V. Conclusion

Design considerations and performance results for low-voltage Si MMIC's including RF and IF amplifiers, Gilbert mixers, and downconverter/upconverter chips developed for mobile and personal communications applications were described. By an optimum selection of bipolar and MOS technologies for different parts in each module, a low-power 2 V operation covering the full frequency range of 1.8–5.2 GHz was realized. The developed modules are expected to find applications in 2 V-class PCS/DECT, ISM-band WAN, Hiperlan systems, and also their dual-mode operation.

Acknowledgment

Thanks are due to K. Maruhashi for his help during noise measurements. The authors are also indebted to M. Nakamae and S. Hasegawa for their support.

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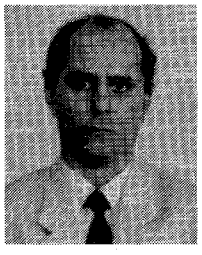

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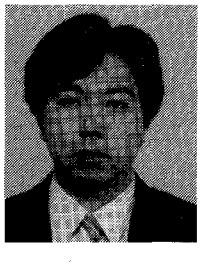

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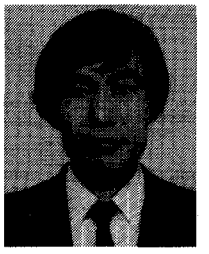

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